Bluetooth™ PA T7023 Design Guide

Please note that information on S-parameters and load-pull data is preliminary.

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General Information

The T7023 is a single supply monolithic SiGe power amplifier designed especially for applications in the 2.4 GHz to 2.5 GHz frequency band. It is especially designed for operation in TDMA systems like Bluetooth, DECT, IEE 802.11 FHSS WLAN, home RF and ISM proprietary radios.

The block diagram of the T7023 is shown in figure 1.

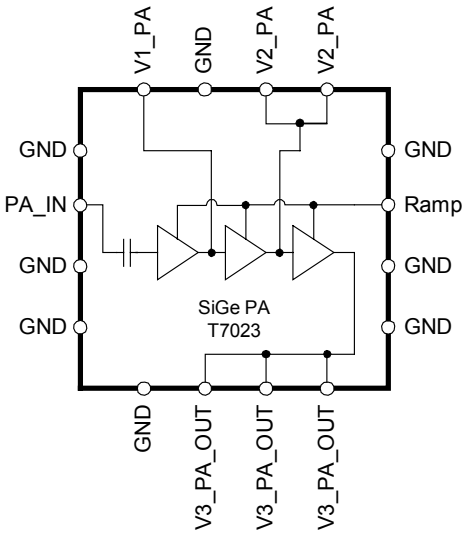

Figure 1. Block diagram

The PA is designed as a three stage amplifier with an analog input control (RAMP) for a simplified control of the output power. This control is also used to switch the PA in a power down mode. The PA is designed to deliver +23dBm (200mW) output power with a power added efficiency of typically 42%.

Reference Design for HP-VFQFP-N16 Package

The typical application module support circuitry of the T7023 in a HP-VFQFP-N16 package is depicted in figures 2, 3 and 4.

The reference design consists of a four-layer FR4 printed circuit board where the two upper layers are used. The layer on the top side contains the RF lines and the DC connections. The internal layers are used for ground connections. The RF lines for the PA input and output are 50 ohm lines with a width of 1 mm and a spacing of 0.5 mm to the ground layer. The two backside layers are connected to ground, however, these layers are not necessary. A Gerber file with information of the printed circuit is available on request.

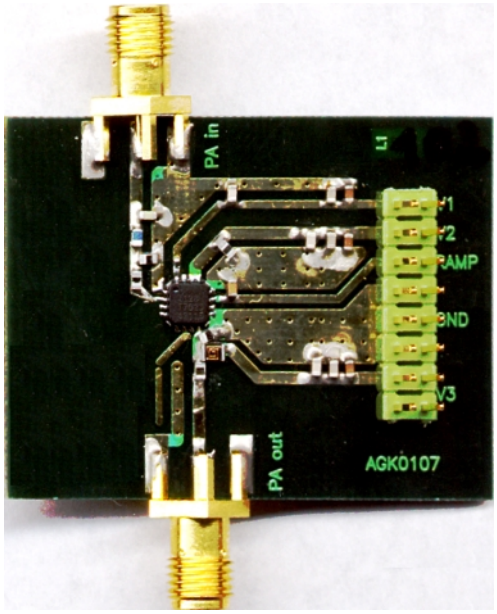

Figure 2. Photograph of the T7023 application board for the HP-VFQFP-N16 package

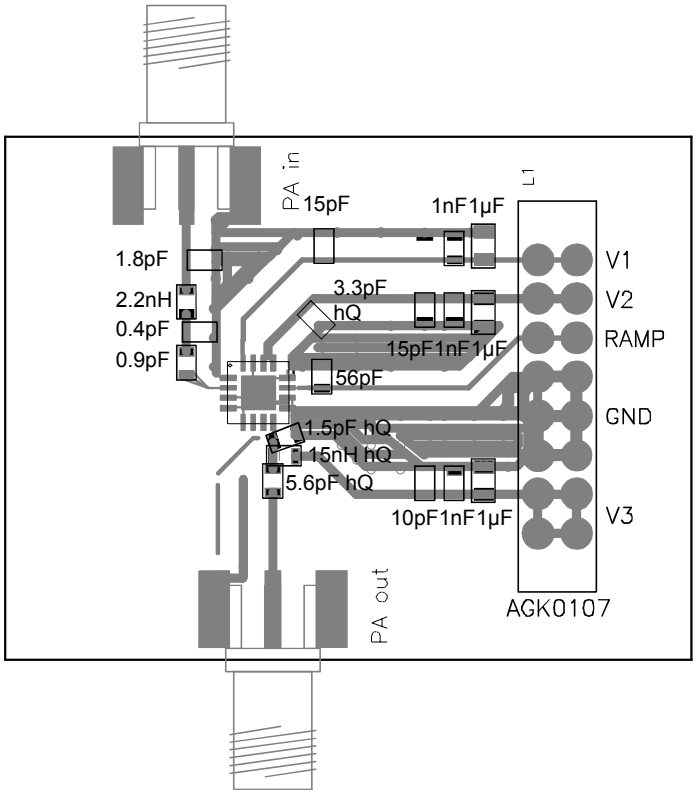

Figure 3. Layout of the T7023 application board for the HP-VFQFP-N16 package

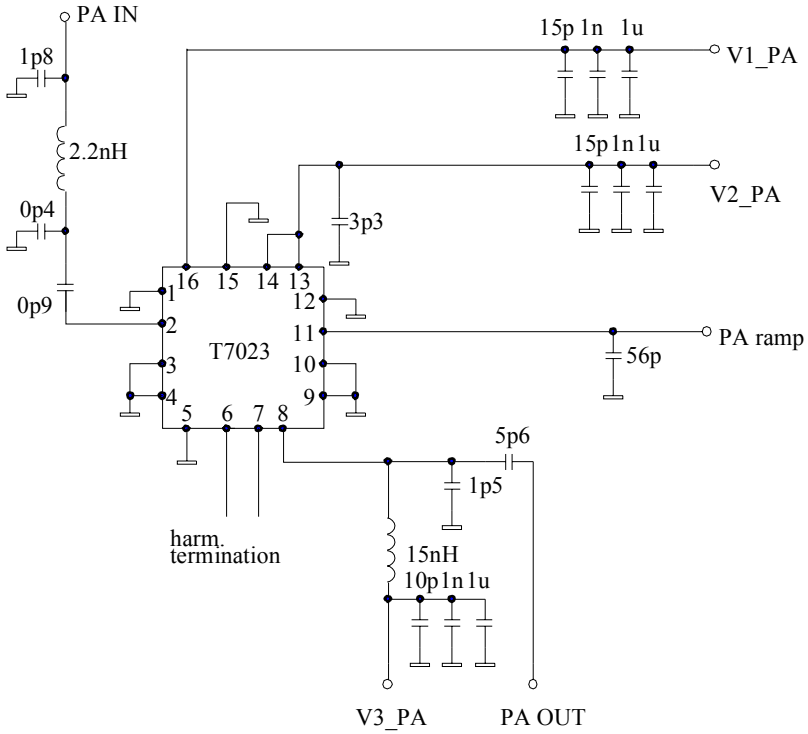

Figure 4. Schematic of the T7023 application board for the HP-VFQFP-N16 package

Power Amplifier

The power amplifier of the T7023 is designed as a three stage amplifier. The input stage of the amplifier is AC coupled to PA_IN, therefore a DC blocking capacitor is not necessary at the input port. However, an external matching circuit should be designed for optimum performance of the power amplifier. The power amplifier has a nominal input power of 0 dBm. It is therefore recommended that the input circuit be designed at this value. This is done for the matching circuits on the application board.

The supply voltage for the collector of the first amplifier stage is connected via V1_PA. Since the collector is internally matched for simplified use of the device, no additional matching is needed.

The supply voltage for the collector of the second stage is fed using a 50 Ohm transmission line. In both reference designs, a capacitor of 3.3 pF with a high Q value should be placed near to the two IC connectors. The RF blocking of this stage with the 15 pF capacitor is done after a length of approx. 10 mm using a 50 Ohm transmission line.

Finally, the third stage uses three output connectors for the open collector. In the reference design for the HP-VFQFP-N16 package, it is recommended that two short stubs with a length of 1 mm be used as a harmonic termination. This harmonic termination is not necessary to achieve the output power, however, a shorting of the second harmonic reduces RF losses in the output transistor and therefore increases the power added efficiency (PAE). For the output matching, a capacitor of 1.5 pF to ground and a DC blocking capacitor of 5.6 pF should be used. Make sure that the capacitor to ground is placed very close to the RF output connectors. The DC feeding inductor of 15 nH should also be placed near to the RF output.

Since the two capacitors in the output matching play the major role for a good match to 50 Ohms, it is recommended that capacitors with a high Q factor be used.

For the design of the output matching circuit it is not correct to use a s-parameter test set or network analyzer. The measurement of the output matching with a network analyzer results in wrong values, since the measurement is done without RF input for the output stage and the output stage is sensitive to RF input power and bias, which also changes with the RF input power. The output matching can only be designed using a load pull setup, with which it is possible to measure the output power vs. load impedance. If a load pull setup is not available, the described matching with two capacitors can be used to transform the output impedance of approx. 22 Ohm +j29 Ohm at 2.4 GHz (at the output pins) to a load of 50 Ohm.

The measured load pull data is summarized in figure 8.

The output matching of the power amplifier includes loads which are used as harmonic terminations. In the schematic, these lines are labeled "harm. termination". The harmonic termination consists of open IC pins, which are internally connected to the PA output. The use of these harmonic terminations results in an increased power added efficiency of the power amplifier. The effect of this harmonic termination influences the output impedance of the power amplifier. These effects are included in the reported reference design.

Please note, that it is important not only to design optimum input and output matching, but also to design the right RF termination at the DC supplies, to get optimum output power and power added efficiency from the PA.

All three stages of the amplifier are separated on the application board allowing access to each collector stage, blocking capacitors are needed on each stage. However, in a final design all blocking functionality can be combined to reduce space and costs.

The output power and the current consumption of the PA is regulated with the ramp connector, which is also used to switch the PA to a standby mode with a low quiescent current typically below 10 µA. A ramp voltage between 1.3 and 1.75 V is the usual operating mode of the power amplifier. A higher ramping voltage results in a higher output power of the PA: The operating point of 23 dBm output power is reached at approx. 1.75 V ramp signal. The ramp control circuit for the T7023 is designed to operate with a control voltage as input signal at the ramp input. However, it is also possible to use a current as an input signal. This has advantages regarding the temperature behavior of the PA. The relation of output power in dependence of ramp current is depicted in the following figure 5.

Application Board Connectors

The application uses two SMA female connectors for the RF signals PA in and PA out. The DC connections are made with one connector for the PA with lines for ramp, ground and the supply voltages for the three amplifier stages V1_PA, V2_PA, and V3_PA.

The connector is depicted in figure 6.

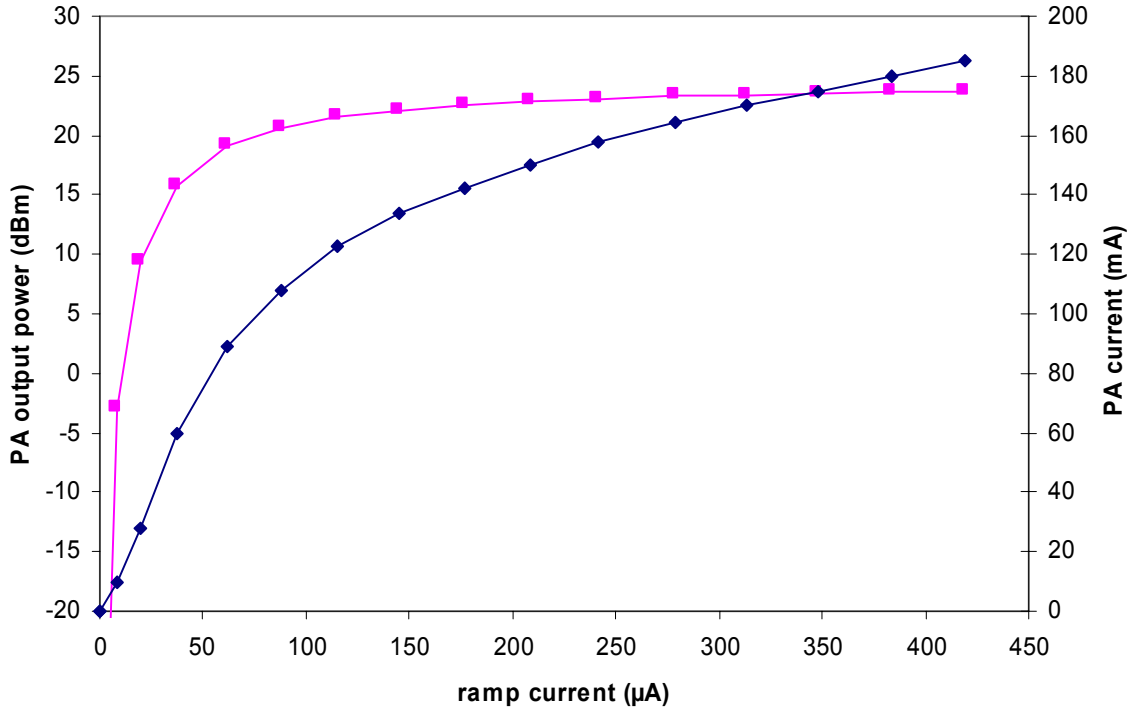

Figure 5. PA output power vs. ramp current

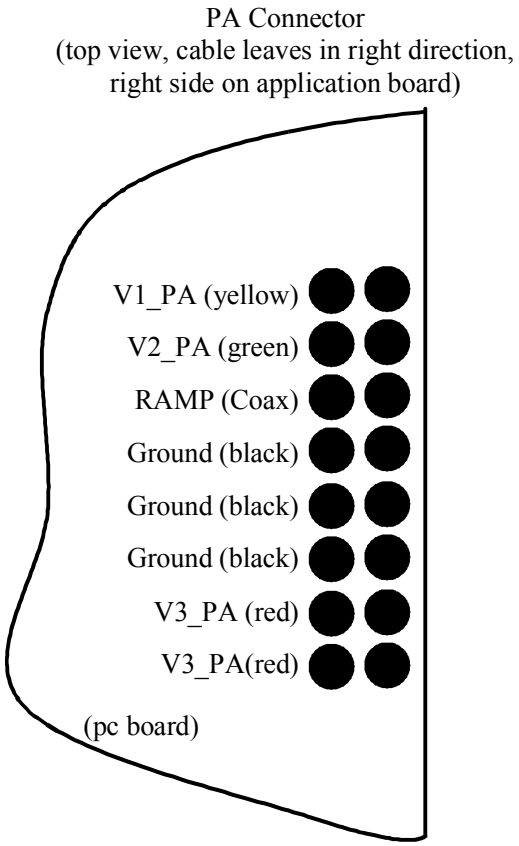

Figure 6. PA connector for application board

S-Parameter Data for the Reference Designs

The following S-parameter diagrams are measured with the described reference designs. However, the reference plane of the calibration is shifted to the input or output pin. The test power for the PA input is 0 dBm.

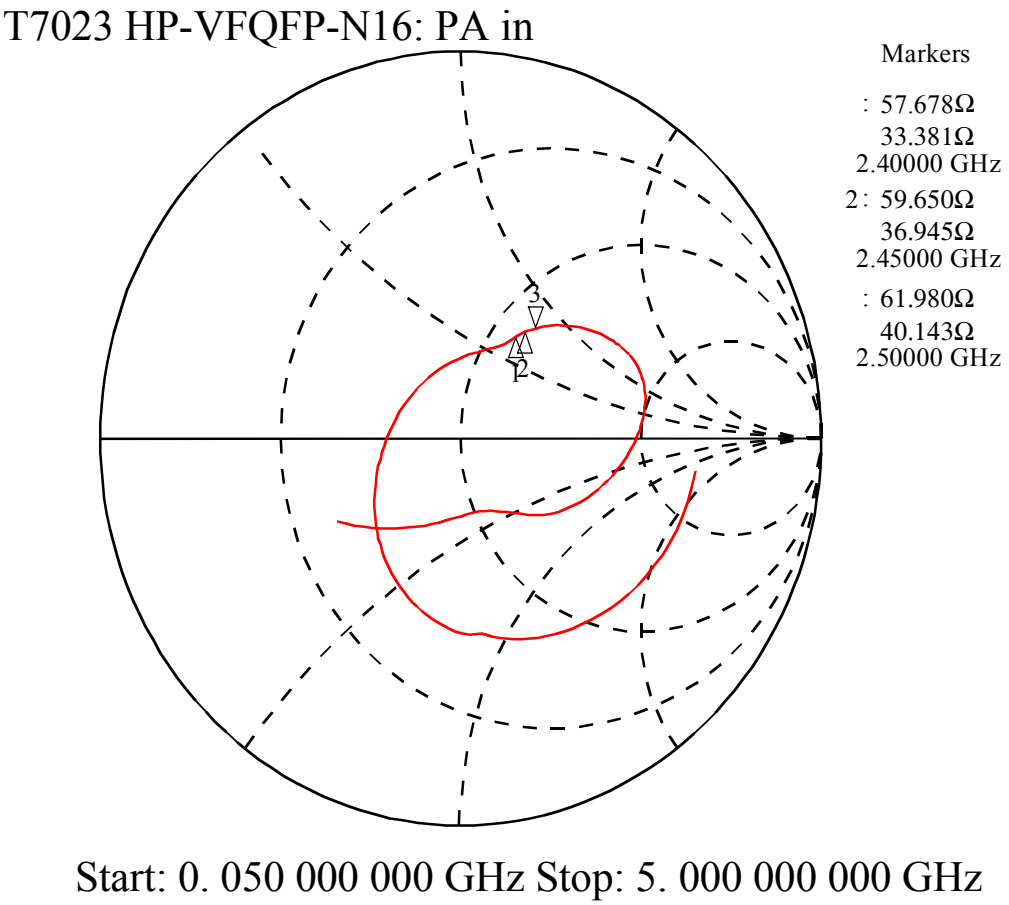

Figure 7. Measured S-parameter data for the PA input

Load Pull Data for the Reference Designs

Load pull measurements of the power amplifiers are made using an ATN load pull system. The measurements were calibrated to the output pins of the power amplifier in order to get the output impedance of the IC. The measurement results are summarized in the following table and in figure 8. The output of the power amplifier uses three pins. However, one pin is used as a harmonic termination. Therefore, during the load pull measurement, the RF load at the two output pins has been changed. The depicted results are the impedances seen by the output transistor for optimum RF power and power added efficiency.

Frequency	HP-VFQFP-N16 package Load impedance
2.4 GHz	22.0 + j 28.6 Ohm
2.45 GHz	19.5 + j 28.8 Ohm
2.48 GHz	16.2 + j 21.4 Ohm
2.5 GHz	14.8 + j 24.7 Ohm

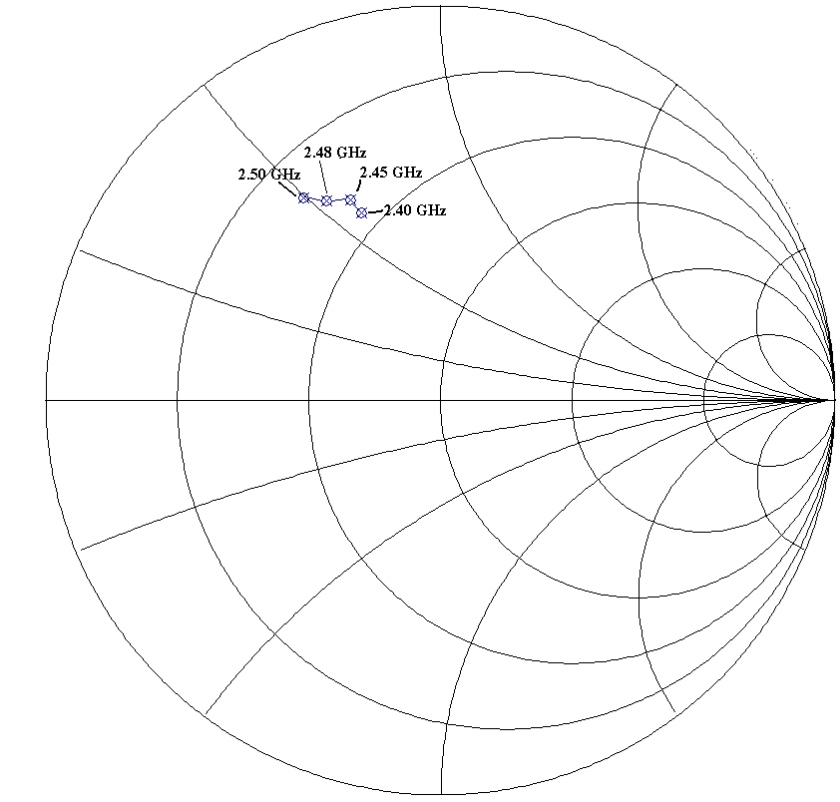

Figure 8. Measured output impedance for the PA output (reference: 50 ohm)