

Preliminary Technical Brief

Wireless Power Management Integrated Circuit

The MC13181 Wireless Power Management Integrated Circuit (PMIC) is a monolithic IC designed for hand-held electronics products in conjunction with the Motorola Bluetooth™ chipset (the MC13180 Bluetooth Radio and MC71000 Bluetooth Protocol Controller) or stand-alone in other products. The MC13181 is ideal for devices operating from a 3.6 V single-cell Lithium-ion battery or other energy systems in the 2.7 to 6.5 V range. The IC features three independently enabled Low Drop Out (LDO) linear voltage regulators for powering baseband, audio, RF/IF, and interface circuitry. A comparator with logic-enabled hysteresis and one scaled input is provided for use as a low-battery detector to protect against destructive battery discharge; it can alternately be used for general system interfacing. A supervisory circuit is integrated to provide a reset signal to the Protocol Controller indicating valid supply. An over-temperature shutdown function is integrated to protect against excessive power dissipation. An IC shutdown input line is provided to allow for disabling of all active circuitry to minimize battery loading and to provide single line master disable. Logic inputs accept V_{ih} levels from 1.5 V to V_{CC} .

Typical Applications

- Add-On Bluetooth Adapter Cards for Cellular Phones
- Cellular Phones
- USB Dongle
- GPS or PDA
- Cordless Headsets
- Other portable devices requiring multiple independent regulators in one package

Features

- Low-Battery Detector
- Three LDO Voltage Regulators
 - 2.55 V, 65 mA for RF/IF
 - 1.85 V, 30 mA for Baseband
 - 3.0/3.3 V, 60 mA for USB, audio CODEC, or other circuitry

MC13181



Package Information

Plastic Package
Case 1307
(QFN-24)

Ordering Information

Device	Operating Temperature Range	Package
MC13181	$T_A = -40$ to 85°C	QFN-24

- Integrated Pass Device
- Independent Enable Lines
- Optimized for Low-Cost Bypass Capacitors
- Microprocessor Supervisor Circuit
- General Purpose Inverter, OR Gate, and Comparator
- Maximum V_{CC} Rated up to 7.0 V
- Voltage-Robust, Level Shifted Logic Inputs to V_{CC} (7.0 V)
- Seamless Integration with Motorola's Bluetooth Chipset

Maximum Ratings

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_I	0 to 7.0	V
Voltage Input	$V_{on/off}$	-0.3 to V_{CC} +0.3	V
Output Voltage	V_{out}	-0.3 to V_{CC} +0.3	V
Output Short Circuit Duration	–	Infinite	–
Thermal Resistance, Junction to Ambient	$R_{\theta ja}$	100	°C/W
Storage Temperature Range	T_{stg}	-40 to 150	°C
Operating Junction Temperature	T_J	125	°C
Lead Soldering Temperature @ 260°C	T_{solder}	10	sec
Power Dissipation		TBD	mW

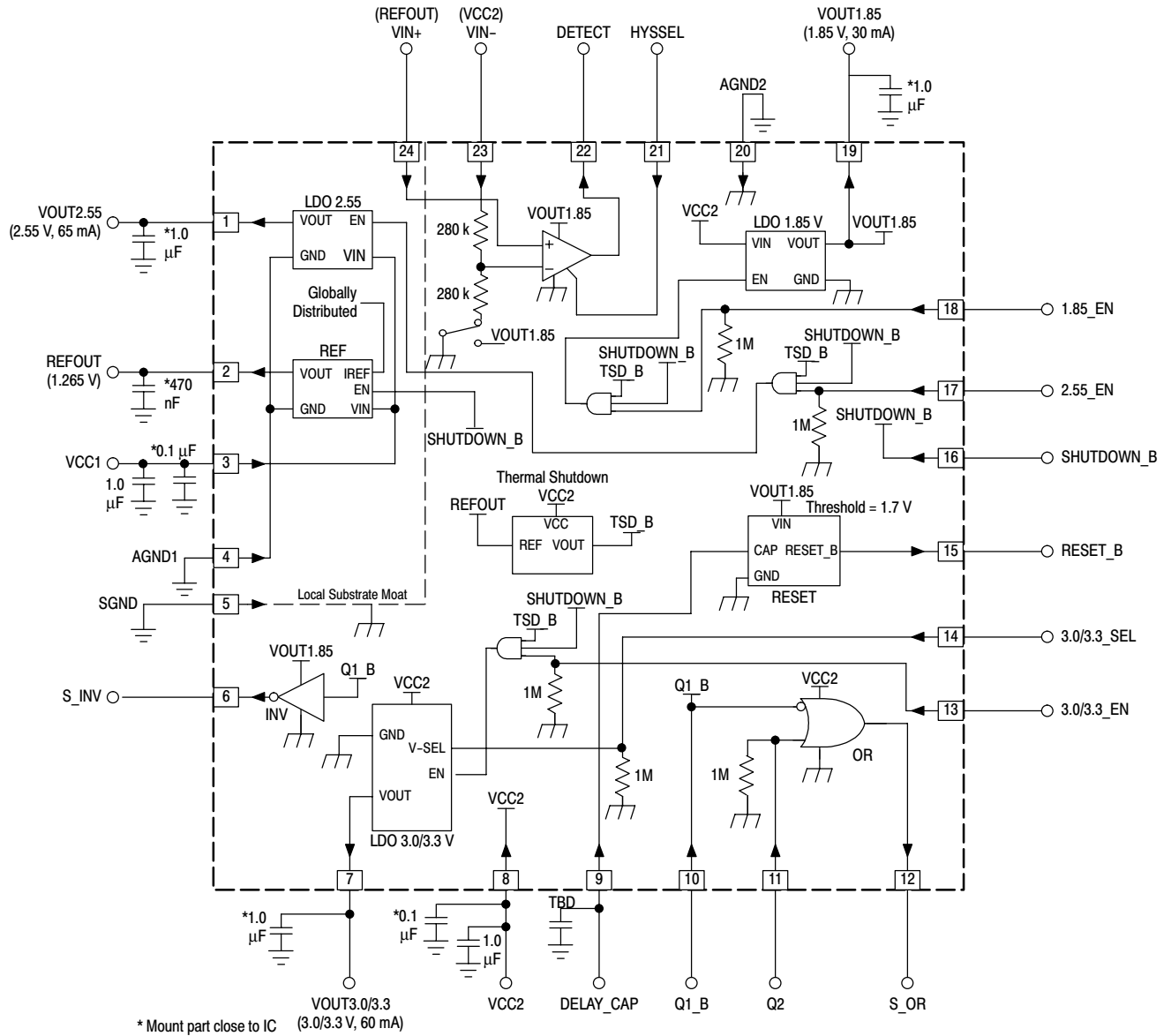
NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Contact Descriptions section.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	–	6.5	V
Operating Temperature	T_A	-40	–	85	°C

1 Block Diagram

Figure 1. Simplified Functional Diagram



2.1 Low Drop Out Regulators (LDO)

2 Circuit Features

2.1 Low Drop Out Regulators (LDO)

The MC13181 incorporates three low drop out regulators. Two of these regulators are fixed voltage. The third regulator is programmable to one of two voltage settings. See Table 1 for voltage and current ratings as well as capacitor requirements.

Table 1. LDO Regulators

LDO	Voltage (V)	Current (mA)	SEL	C byp (μ F)
1	1.85	30	–	1.0
2	2.55	65	–	1.0
3	3.0	60	high	1.0
3	3.3	60	low	1.0

All three regulators are designed for use with low-value, low-cost bypass capacitors. Low ESR tantalum capacitors are recommended (high performance ceramic capacitors with extremely low ESR, $\ll 1\Omega$, should be avoided at regulator outputs to ensure stability). Additional filter capacitors should be placed across each V_{CC} input.

All three regulators are designed for high Power Supply Rejection Ratio (PSRR), low standby current, good line and load regulation, and fast turn on.

The first regulator, LDO 1.85 V, supplies 1.85 V. It is capable of a nominal output current of 30 mA. This regulator is ideal for powering low-voltage digital or baseband circuitry.

The second regulator, LDO 2.55 V, supplies 2.55 V at up to 65 mA. This regulator is intended to supply power for RF/IF circuitry. This regulator is optimized for slightly better close-in PSRR performance.

The third regulator, LDO 3.0/3.3 V, can be set to either 3.0 V out to 3.3 V out through a single select line. The output can source 60 mA. This regulator can be used to supply USB power or power some other peripheral as needed. If the input voltage drops below the overhead needed for regulation, the output of this regulator will track the input down to 2.7 V.

All three regulators have an external active-high enable line.

2.2 Reference Regulator

The Reference Regulator supplies a precise 1.265 V for use by the other on-chip regulators. To maintain spectral purity on the LDO regulators, this internal reference is not intended for external loading. A contact is provided for an off-chip 0.47 μ F capacitor for bypassing.

2.3 Shutdown

The active-low shutdown input disables all regulators and logic.

2.4 Reset Circuit

The RESET_B output goes high after a delay, based on the delay capacitor. It is initiated when LDO 1.85 V rises above the reset threshold. When LDO 1.85 V falls below the reset threshold, RESET_B goes low with no delay.

2.5 Comparator with Programmable Hysteresis

The MC13181 includes a general purpose comparator. The V_{IN-} input to the IC connects to internal scaling resistors coupling a scaled (by a factor of approximately 0.44) voltage to the minus input of the comparator. The V_{IN+} input is directly connected to the plus input of the comparator. Although one input has a fixed divider ratio, the comparator may be used for general purpose applications. A typical application connects the V_{IN-} input to V_{CC} and V_{in+} to REFOUT for Under-Voltage Detection at 2.88 V with no additional components required.

The hysteresis, of typically 30 mV, can be enabled or disabled via the HYSSEL contact.

The output of the comparator is push-pull referenced to LDO 1.85 V. The input range is referenced to V_{CC} .

2.6 OR Gate & Inverter

The IC incorporates a general purpose inverter and OR gate. The Q1_B input is the input to the inverter and one of the OR gate inputs. The S_inv output will be the logical inversion of the input. The S_OR output will be the logical OR of Q1_B and Q2. Q2 has an internal pull-down.

Both inputs feature voltage robust level shifting and a V_{ih} may range from 1.5 V through V_{CC} . The inverter output is referenced to LDO 1.85 V, the OR gate output is referenced to V_{CC} .

2.7 Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC and system in the event that the maximum junction temperature is exceeded. When activated (typical threshold is set at 150°C), the three LDO regulators turn off until they are reactivated. This feature is provided to prevent failures from accidental overheating. Hysteresis will be implemented to allow stable thermal recovery.

Care should be taken to ensure that regulator loading and ambient thermal conditions are managed to avoid excessive power dissipation and thermal shutdown in operation.

PC Board layout should include connection to exposed thermal pad on IC and ensure adequate heat dissipation.

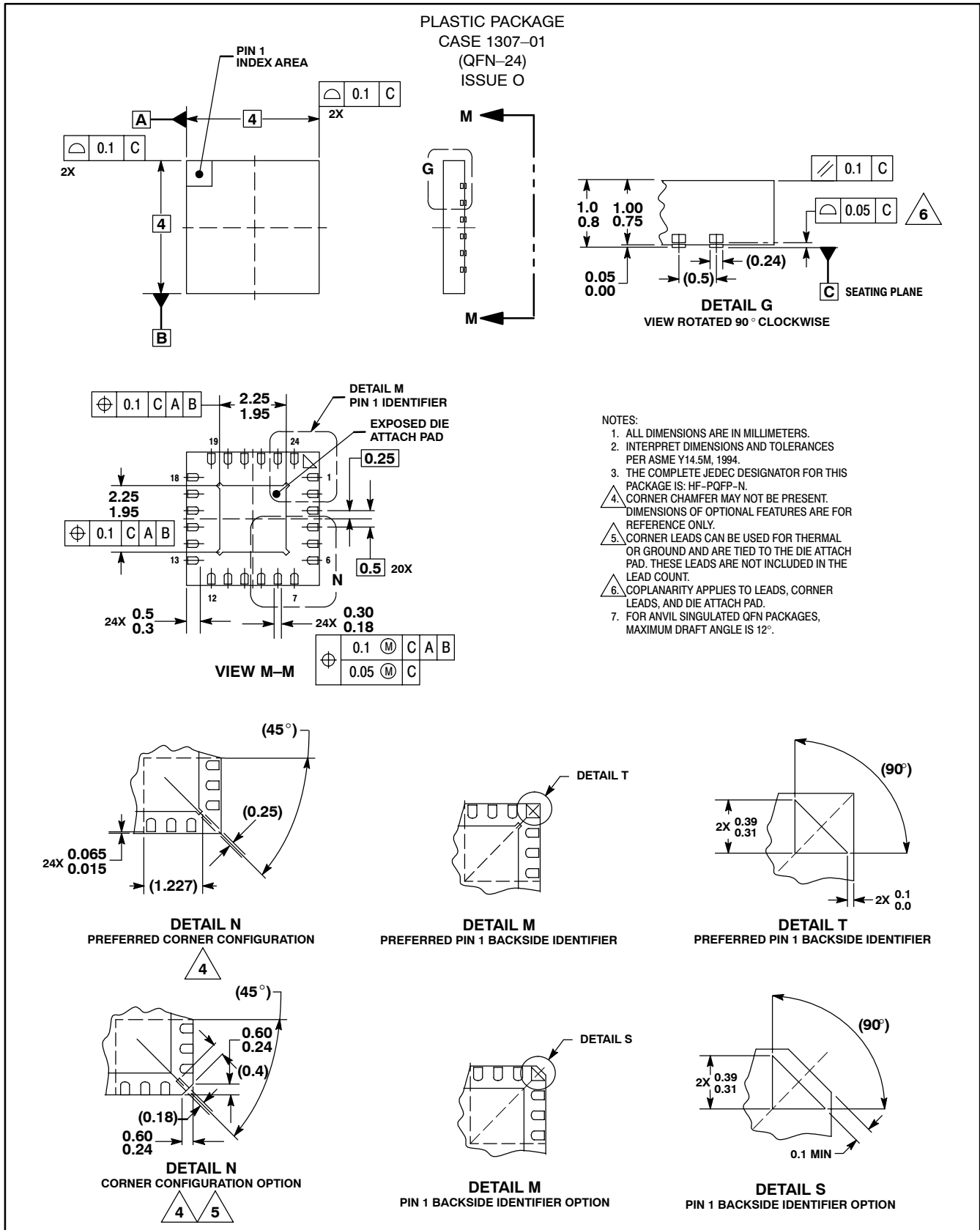
Table 2. Contact Definitions

Contact	Name	Description
1	VOUT2.55	LDO 2.55 V Output, Bypass with low ESR 1.0 μ F tantalum capacitor [Note 1]
2	REFOUT	1.25 V Reference Voltage Output, Bypass with low ESR 470 nF capacitor [Note 1]
3	VCC1	Power Supply Input for Reference Generation and LDO 2.55 V
4	AGND1	Analog Ground for Reference Generation and LDO 2.55 V
5	SGND	Substrate for LDO 2.55 and Reference Generator; tie to ground
6	S_INV	Inverter Output
7	VOUT3.0/3.3	LDO 3.0 / 3.3 V Output, Bypass with low ESR 1.0 μ F tantalum capacitor [Note 1]
8	VCC2	Power Supply Input for non- V_{CC1} blocks
9	DELAY_CAP	Reset Delay Cap Input
10	Q1_B	Input to Inverter and Complementary Input to OR Gate
11	Q2	OR Input
12	S_OR	OR Output
13	3.0/3.3_EN	LDO 3.0 / 3.3 V Enable
14	3.0/3.3_SEL	Input logic control for 3.0 or 3.3 V from LDO 3.0 / 3.3 V
15	RESET_B	Reset Push-Pull Output
16	SHUTDOWN_B	Single contact Master Disable, Low = IC Shutdown
17	2.55_EN	LDO 2.55 V Enable
18	1.85_EN	LDO 1.85 V Enable
19	VOUT1.85	LDO 1.85 V Output, Bypass with low ESR 1.0 μ F tantalum capacitor [Note 1]
20	AGND2	Analog Ground
21	HYSSEL	Input logic control for Comparator Hysteresis
22	DETECT	Comparator Push-Pull Output
23	VIN-	Inverting Input to Comparator through divider string
24	VIN+	Non-inverting Input to Comparator

NOTES: 1. All capacitors are assumed to be low ESR tantalum. De-rating factor on capacitance value is assumed to be -20% to 10% over all cases of tolerance and temperature.
2. Contact assignments are subject to change.

3 Packaging

Figure 2. Outline Dimensions



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